

Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 7 with the following amended paragraph:

FIG. 2 is a graph [[of]] illustrating tolerances used in the method performed by the CMP system.

Please replace the paragraph beginning at page 5, line 10 with the following amended paragraph:

FIG. 5 is a ~~flowcharts~~ flowchart illustrating a conventional polishing control method.

Please replace the paragraph beginning at page 10, line 3 with the following amended paragraph:

Initially, the gating wafer is extracted from the cassette, run through the polishing apparatus, and directed to the in-line metrology device (step 402). While the gating wafer is being processed, the rest of the substrates are not processed. If the resulting layer thickness on the first gating wafer is outside ~~within~~ the specification limits or the target limits, the polishing time is adjusted, and the next substrate in the cassette is classified as a second gating wafer, extracted from the cassette, run through the polishing apparatus, and directed to the in-line metrology device (steps 404 and 406). The control system continues to classify substrates as gating wafers until one has a layer thickness within the target limits (step 406). At this point, the previously calculated polishing time is set as the default polishing time (step 408), and polishing of the rest of the substrates from the cassette can commence, with multiple substrates passing through the CMP system simultaneously.